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09/781,982	02/14/2001	Akira Itoh	L7016.01102	9554

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EXAMINER	
THOMPSON, JAMES A	

ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/781,982	ITOH, AKIRA	
	Examiner	Art Unit	
	James A. Thompson	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 7, lines 4-7, filed 15 December 2004, with respect to the rejections under 35 USC §112, second paragraph have been fully considered and are persuasive. The rejections under 35 USC §112, second paragraph listed in items 2-3 of the previous office action, dated 15 September 2004 have been withdrawn.

2. Applicant's arguments filed 15 December 2004 have been fully considered but they are not persuasive.

Regarding page 7, line 11 to page 9, line 3: Examiner has cited more than just column 7, lines 23-27 of Zhou (US Patent 5,798,753) to teach converting parallel image data to serial image data. Specifically, Examiner stated in said previous office action "a plurality of image processing means (figure 4 (406A,406B,406C,406D) of Zhou) for converting parallel image data inputted from said image input connection means (column 6, line 67 to column 7, line 8 of Zhou) to serial image data (column 7, lines 23-27 of Zhou), said plurality of image processing means being provided respectively in association with a plurality of development colors (column 7, lines 16-22 of Zhou)." The individual color image components, and thus four different sets of image data, are processed in parallel with parallel processors (figure 4(406A,406B,406C,406D) and column 6, line 67 to column 7, line 8 of Zhou) and are then output as 4:2:0 YUV format color image data (column 7, lines 23-27 of Zhou). The 4:2:0 YUV format is output to an output device. Even if there were a plurality of output devices, the data

itself is serial image data since it is now in a single, combined format. The "multiplication, addition, scaling and clipping operations" [page 7, lines 1-4 of present arguments] that Applicant mentions are operations that are performed *in parallel* to each color component before the data is combined into a single combined, and thus serial, color image format.

Regarding page 9, line 4 to end of page 9: The rejections regarding the newly added claim 4 are given in detail below.

Regarding page 10, line 1 to page 11, line 3: Examiner has not suggested in said previous office action that a mere change in binary representation (zero/one as opposed to one/zero) is the motivation to combine Tachiuchi (US Patent 4,839,739) with Zhou, nor does the cited passage of Tachiuchi teach or suggest such a feature. The motivation, as clearly set forth in said previous office action, states that the clock taught by Tachiuchi is combinable since the *frequency* of the clock signals affects how the image signal is binarized. The variable frequency feature of the clocks is combinable since each color is processed in parallel and can thus be processed according to different frequencies.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou (US Patent 5,798,753) in view of Tachiuchi (US 4,839,739).

Regarding claim 1: Zhou discloses an image processing apparatus (figure 7 of Zhou) comprising central processing means (figure 7(24) of Zhou) for conducting operation control of the whole image processing apparatus (column 3, lines 49-52 of Zhou); setting means (figure 7(52) of Zhou) for storing control information specified by said central processing means (column 7, lines 4-8 and column 11, lines 20-22 of Zhou); image input connection means (figure 7(54) of Zhou) for receiving predetermined data from an external device (column 11, lines 8-15 of Zhou); and a plurality of image processing means (figure 4 (406A,406B,406C,406D) of Zhou) for converting parallel image data inputted from said image input connection means (column 6, line 67 to column 7, line 8 of Zhou) to serial image data (column 7, lines 23-27 of Zhou), said plurality of image processing means being provided respectively in association with a plurality of development colors (column 7, lines 16-22 of Zhou). The parallel processing is performed to produce a resultant color image (column 7, lines 23-27 of Zhou), said color image being inherently serial image data since said color image data is output to a single output device (figure 7(58A) and column 11, lines 14-17 of Zhou).

Zhou further discloses image output connection means (figure 7(56) of Zhou) for transferring the serial image data (column 11, lines 2-4 of Zhou) to an external device (figure 7 (58A) and column 11, lines 14-17 of Zhou).

Zhou does not disclose expressly clock generation means for generating a clock signal having a basic period equivalent to

that of a pixel or less; a plurality of variable frequency generation means for adjusting a frequency of the clock signal outputted from said clock generation means to a predetermined level independently of each other, based on the control information specified by said central processing means, said plurality of variable frequency generation means being provided respectively in association with a plurality of development colors; and that each of said plurality of image processing means converts said parallel image data based on a frequency of a clock signal outputted from associated one of said variable frequency generation means.

Tachiuchi discloses clock generation means (figure 10(21) of Tachiuchi) for generating a clock signal (column 6, lines 56-58 of Tachiuchi) having a basic period equivalent to that of a pixel or less (column 4, lines 23-26 of Tachiuchi). The frequency of the input signal of the amplifier (column 4, lines 17-23 of Tachiuchi) is used to generate the binary signal pixel data (column 4, lines 23-26 of Tachiuchi). Said frequency is taken from the original frequency of the oscillator, which is then divided (column 6, lines 56-58 of Tachiuchi). Since the frequency of the input signal of the amplifier is used to generate the binary signal pixel data, the frequency of the oscillator must inherently have a frequency equivalent to that of a pixel or more. Otherwise, said frequency will be too slow to sample the pixel data. Since, as is well known in the art, frequency (f) is the inverse of the period (T) ($T=\frac{1}{f}$), then the basic period of said generated clock signal is equivalent to that of a pixel or less.

Tachiuchi further discloses a plurality of variable frequency generation means (figure 2(10) and column 7, lines 27-32 of Tachiuchi) for adjusting a frequency of the clock signal outputted from said clock generation means (column 3, lines 65 to column 4, line 1 of Tachiuchi) to a predetermined level (column 3, lines 62-65 of Tachiuchi). Since the individual circuit are used for each of a plurality of colors (column 7, lines 27-32 of Tachiuchi), said frequencies of each color are therefore adjusted independently of each other. Said frequencies are adjusted based on the control information specified by a central processing means (figure 2(11) and column 3, lines 65-68 of Tachiuchi). Said plurality of variable frequency generation means is provided respectively in association with a plurality of development colors (column 7, lines 27-32 of Tachiuchi).

Tachiuchi further discloses converting each color of the image data based on a frequency of a clock signal outputted from the variable frequency generation means (column 4, lines 8-12 and lines 17-23 of Tachiuchi).

Zhou and Tachiuchi are combinable because they are from the same field of endeavor, namely digital image data generation and processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to generate a clock signal with a basic period equivalent to that of a pixel or less, as taught by Tachiuchi. The motivation for doing so would have been that such a signal is necessary for inputting and binarizing image data since the frequency of said signal can affect how the image data is binarized (column 4, lines 23-26 of Tachiuchi). Further, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to

use each the plurality of variable frequency generation means taught by Tachiuchi respectively for each of the parallel processed colors taught by Zhou. Since each color is processed separately and in parallel according to the teachings of Zhou (column 7, lines 12-22 of Zhou), a separate variable frequency generation means would be required for each color, which would further result in each color of the parallel image data being processed based on the associated one of the plurality of variable frequency generation means. The motivation for doing so would have been that each color has different characteristics (figure 14 and column 7, lines 58-62 of Tachiuchi) and can therefore be handled separately of each other (column 7, lines 62-65 of Tachiuchi). Therefore, it would have been obvious to combine Tachiuchi with Zhou to obtain the invention as specified in claim 1.

Regarding claim 4: Zhou discloses a plurality of image processors (figure 4(406A,406B,406C,406D) of Zhou) that each convert parallel image data (column 6, line 67 to column 7, line 8 of Zhou) to serial image data (column 7, lines 23-27 of Zhou), said plurality of image processing means being provided respectively in association with a plurality of development colors (column 7, lines 16-22 of Zhou). The parallel processing is performed to produce a resultant color image (column 7, lines 23-27 of Zhou), said color image being inherently serial image data since said color image data is output to a single output device (figure 7(58A) and column 11, lines 14-17 of Zhou).

Zhou does not disclose expressly a plurality of variable frequency generators, each corresponding to a different one of a plurality of development colors, that separately generate clock signals of desired frequencies; that said plurality of image

processors each correspond to a respective one of said variable frequency generators; that said parallel image data is converted to *variable resolution* serial image data based on the frequency of the associated clock signal, wherein for each image processor, the frequency of the associated clock signal determines the degree of resolution the converted serial image data represents with respect to the corresponding parallel image data.

Tachiuchi discloses a plurality of variable frequency generators (figure 2(10) and column 7, lines 27-32 of Tachiuchi). Since each of the individual circuits are used for each of a plurality of colors (column 7, lines 27-32 of Tachiuchi), said frequencies of each color are therefore adjusted independently of each other, and thus separately generate clock signals of desired frequencies. Said frequencies are adjusted based on the control information specified by a central processing means (figure 2(11) and column 3, lines 65-68 of Tachiuchi). Said plurality of variable frequency generation means is provided respectively in association with a plurality of development colors (column 7, lines 27-32 of Tachiuchi).

Tachiuchi further discloses converting each color of the image data based on a frequency of a clock signal outputted from the variable frequency generation means (column 4, lines 8-12 and lines 17-23 of Tachiuchi).

Tachiuchi further discloses that the image data is converted to variable resolution image data (column 4, lines 20-28 of Tachiuchi) based on the frequency of the associated clock signal (column 4, lines 8-12 and lines 17-23 of Tachiuchi). The frequency of the associated clock signal determines the degree of resolution the converted image data represents with respect

to the corresponding original image data (figures 5A-5B; figures 6A-6B; and column 4, lines 23-27 of Tachiuchi). Since f_2 (figures 6A-6B of Tachiuchi) is twice the frequency of f_1 (figures 5A-5B of Tachiuchi), the number of "1" bits in the binary signal is less for f_2 (000011) than for f_1, (001111) and thus the resolution of the image signal is finer spatially. Further, a higher spatial resolution is precisely what one of ordinary skill in the art would expect to result from a higher corresponding clock frequency since, as is well-known in signal processing, a higher sampling frequency generates a higher data rate. Thus, the variable resolution of the image data is naturally based upon the frequency of the associated clock.

Zhou and Tachiuchi are combinable because they are from the same field of endeavor, namely digital image data generation and processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use each the plurality of variable frequency generation means taught by Tachiuchi respectively for each of the parallel processed colors taught by Zhou. Since each color is processed separately and in parallel according to the teachings of Zhou (column 7, lines 12-22 of Zhou), a separate variable frequency generation means would be required for each color, which would further result in each color of the parallel image data being processed based on the associated one of the plurality of variable frequency generation means. Further, due to the variable resolution resulting from each of the individual clock signals, said parallel image data is therefore converted to variable resolution serial image data based on the frequency of the associated clock signal, wherein for each image processor, the frequency of the associated clock signal determines the degree

of resolution the converted serial image data represents with respect to the corresponding parallel image data. The motivation for doing so would have been that each color has different characteristics (figure 14 and column 7, lines 58-62 of Tachiuchi) and can therefore be handled separately of each other (column 7, lines 62-65 of Tachiuchi). Therefore, it would have been obvious to combine Tachiuchi with Zhou to obtain the invention as specified in claim 4.

5. Claims 2-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou (US Patent 5,798,753) in view of Tachiuchi (US 4,839,739) and Bianchi (US Patent 5,898,509).

Regarding claim 2: Zhou discloses an image processing apparatus (figure 7 of Zhou) comprising central processing means (figure 7(24) of Zhou) for conducting operation control of the whole image processing apparatus (column 3, lines 49-52 of Zhou); setting means (figure 7(52) of Zhou) for storing control information specified by said central processing means (column 7, lines 4-8 and column 11, lines 20-22 of Zhou); image input connection means (figure 7(54) of Zhou) for receiving predetermined data from an external device (column 11, lines 8-15 of Zhou); a plurality of image processing means (figure 4 (406A,406B,406C,406D) of Zhou) for converting parallel image data inputted from said image input connection means (column 6, line 67 to column 7, line 8 of Zhou) to serial image data (column 7, lines 23-27 of Zhou), said plurality of image processing means being provided respectively in association with all development colors (column 7, lines 16-22 of Zhou). The parallel processing is performed to produce a resultant color image (column 7, lines 23-27 of Zhou), said color image being

inherently serial image data since said color image data is output to a single output device (figure 7(58A) and column 11, lines 14-17 of Zhou).

Zhou further discloses image output connection means (figure 7(56) of Zhou) for transferring the serial image data (column 11, lines 2-4 of Zhou) to an external device (figure 7 (58A) and column 11, lines 14-17 of Zhou).

Zhou does not disclose expressly clock generation means for generating a clock signal having a basic period equivalent to that of a pixel or less; a plurality of variable frequency generation means for adjusting a frequency of the clock signal outputted from said clock generation means to a predetermined level independently of each other, based on the control information specified by said central processing means, said plurality of variable frequency generation means being provided respectively in association with development colors other than one predetermined color; and that each of said plurality of image processing means converts said parallel image data based on a frequency of the clock signal outputted from said clock generation means and a frequency of a clock signal outputted from associated one of said variable frequency generation means by taking the frequency of the clock outputted from the clock generation means as a reference.

Tachiuchi discloses clock generation means (figure 10(21) of Tachiuchi) for generating a clock signal (column 6, lines 56-58 of Tachiuchi) having a basic period equivalent to that of a pixel or less (column 4, lines 23-26 of Tachiuchi). The frequency of the input signal of the amplifier (column 4, lines 17-23 of Tachiuchi) is used to generate the binary signal pixel data (column 4, lines 23-26 of Tachiuchi). Said frequency is

taken from the original frequency of the oscillator, which is then divided (column 6, lines 56-58 of Tachiuchi). Since the frequency of the input signal of the amplifier is used to generate the binary signal pixel data, the frequency of the oscillator must inherently have a frequency equivalent to that of a pixel or more. Otherwise, said frequency will be too slow to sample the pixel data. Since, as is well known in the art, frequency (f) is the inverse of the period (T) ($T=\frac{1}{f}$), then the basic period of said generated clock signal is equivalent to that of a pixel or less.

Tachiuchi further discloses a plurality of variable frequency generation means (figure 2(10) and column 7, lines 27-32 of Tachiuchi) for adjusting a frequency of the clock signal outputted from said clock generation means (column 3, lines 65 to column 4, line 1 of Tachiuchi) to a predetermined level (column 3, lines 62-65 of Tachiuchi). Since the individual circuit are used for each of a plurality of colors (column 7, lines 27-32 of Tachiuchi), said frequencies of each color are therefore adjusted independently of each other. Said frequencies are adjusted based on the control information specified by a central processing means (figure 2(11) and column 3, lines 65-68 of Tachiuchi). Said plurality of variable frequency generation means is provided respectively in association with a plurality of development colors (column 7, lines 27-32 of Tachiuchi).

Tachiuchi further discloses converting each color of the image data based on a frequency of a clock signal outputted from the variable frequency generation means (column 4, lines 8-12 and lines 17-23 of Tachiuchi).

Zhou and Tachiuchi are combinable because they are from the same field of endeavor, namely digital image data generation and processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to generate a clock signal with a basic period equivalent to that of a pixel or less, as taught by Tachiuchi. The motivation for doing so would have been that such a signal is necessary for inputting and binarizing image data since the frequency of said signal can affect how the image data is binarized (column 4, lines 23-26 of Tachiuchi). Further, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the variable frequency generation means taught by Tachiuchi respectively for each of the parallel processed colors taught by Zhou. Since each color is processed separately and in parallel according to the teachings of Zhou (column 7, lines 12-22 of Zhou), a separate variable frequency generation means would be required for each color, which would further result in each color of the parallel image data being processed based on the associated one of the plurality of variable frequency generation means. The motivation for doing so would have been that each color has different characteristics (figure 14 and column 7, lines 58-62 of Tachiuchi) and can therefore be handled separately of each other (column 7, lines 62-65 of Tachiuchi). Therefore, it would have been obvious to combine Tachiuchi with Zhou.

Zhou in view of Tachiuchi does not disclose expressly that said plurality of variable frequency generation means is provided in association with development colors other than one predetermined color; and that said parallel image data is converted based on a frequency of the clock signal outputted

from said clock generation means and a frequency of a clock signal outputted from associated one of said variable frequency generation means by taking the frequency of the clock signal outputted from the clock generation means as a reference.

Bianchi discloses that the weakest channel determines the overall cycle time (column 6, lines 10-12 of Bianchi). The other channels are variably set using the cycle time of the weakest channel as a reference (column 6, lines 14-17 of Bianchi). Therefore, the cycle time for the weakest channel is set to a constant, reference value (column 6, lines 10-14 of Bianchi), and the other channels are independently set based on said reference value (column 6, lines 14-17 of Bianchi). The cycle time (T) inversely relates to the frequency (f) since, as is well-known in the art, $T=\frac{1}{f}$. Therefore, setting a reference cycle time inherently set a reference frequency, and variably setting other cycle times based on said reference cycle time inherently sets frequencies based on said reference frequency.

Zhou in view of Tachiuchi is combinable with Bianchi because they are from the same field of endeavor, namely digital image data generation and processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to set one channel as a reference channel for the cycle time and set the cycle times of the other channels based on said reference cycle time, as taught by Bianchi. Therefore, there would be no need for a variable frequency generation means for one predetermined color, namely the color that requires a longer cycle time than the other colors. The frequency of the clock signal outputted from said clock generation means would correspond to the frequency of the

reference channel (color). Therefore, the frequencies of the clock signals outputted from their associated variable frequency generation means would be determined by taking the frequency of the clock signal outputted from the clock generation means as a reference. The motivation for doing so would have been that the maximum and minimum light intensities at the CCD may be different for one color band than for another color band (column 1, lines 51-53 of Bianchi) and therefore parameters, such as the clock cycle time, must be adjusted to maximize the signal-to-noise ratio (column 1, lines 56-58 of Bianchi). Therefore, it would have been obvious to combine Bianchi with Zhou in view of Tachiuchi to obtain the invention as specified in claim 2.

Regarding claim 3: Zhou discloses that said central processing means has control information to control at least one of the processing operation of said plurality of image processing means and the frequency adjusting operation of said variable frequency generation means (column 7, lines 4-8 and column 11, lines 20-22 of Zhou). Said plurality of image processing means operate according to the scale factor stored in the scale factor register (column 7, lines 4-8 of Zhou), which is controlled by said central processing means since said central processing means controls the color conversion processing (column 11, lines 20-22 of Zhou) and the overall operation of the device (column 3, lines 49-52 of Zhou).

Zhou in view of Tachiuchi does not disclose expressly that said plurality of image processing means are adapted to conduct image addition/removal processing operation.

Bianchi discloses conducting an image addition/removal processing operation (column 3, lines 31-37 of Bianchi). The DUMP operation of the CCD takes the charges that have collected

due to the addition of image data (column 3, lines 35-37 of Bianchi), and transfers said charges to an analog shift register (column 3, lines 31-33 of Bianchi), thus initializing the CCD cells (column 3, lines 33-34 of Bianchi).

Zhou in view of Tachiuchi is combinable with Bianchi because they are from the same field of endeavor, namely digital image data generation and processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the DUMP operation taught by Bianchi as part of the operation of said image processing apparatus. The motivation for doing so would have been to clear the image data memory so that more image data can be processed by said image processing apparatus (column 3, lines 35-37 of Bianchi). Therefore, it would have been obvious to combine Bianchi with Zhou in view of Tachiuchi to obtain the invention as specified in claim 3.

Regarding claim 5: The arguments regarding claim 4 are incorporated herein.

Bianchi discloses that the weakest channel determines the overall cycle time (column 6, lines 10-12 of Bianchi). The other channels are variably set using the cycle time of the weakest channel as a fixed-rate reference (column 6, lines 14-17 of Bianchi). Therefore, the cycle time for the weakest channel is set to a fixed, reference value (column 6, lines 10-14 of Bianchi), and the other channels are independently set based on said reference value (column 6, lines 14-17 of Bianchi). The cycle time (T) inversely relates to the frequency (f) since, as is well-known in the art, $T=\frac{1}{f}$. Therefore, setting a reference cycle time inherently set a reference frequency, and variably

setting other cycle times based on said reference cycle time inherently sets frequencies based on said reference frequency.

Zhou in view of Tachiuchi is combinable with Bianchi because they are from the same field of endeavor, namely digital image data generation and processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to set one channel, which would correspond to one of the plurality of development colors taught by Zhou, as a fixed-rate reference channel for the cycle time and set the cycle times of the other channels based on said reference cycle time, as taught by Bianchi. Therefore, one of the frequency generators would instead be a fixed-rate frequency generator, which also corresponds to a different one of the plurality of development colors, that separately generates a clock signal of a desired frequency. Further, the image processor associated with color channel controlled by said fixed-rate frequency generator would therefore be another image processor, associated with the same development color as the fixed-rate frequency generator, that converts parallel image data to serial image data based on the frequency of the fixed-rate frequency generator's clock signal, wherein the frequency of the clock signal of the fixed-rate generator determines the degree of resolution the converted serial image data represents with respect to the corresponding parallel image data. In short, by converting one of the plurality of variable frequency generators into the fixed-rate frequency generator taught by Bianchi which the remaining variable frequency generators reference for their frequency value, each and every limitation of claim 5 has been rendered unpatentable due to be obvious over Zhou in view of Tachiuchi and Bianchi. The motivation for combining Bianchi

with Zhou in view of Tachiuchi would have been that the maximum and minimum light intensities at the CCD may be different for one color band than for another color band (column 1, lines 51-53 of Bianchi) and therefore parameters, such as the clock cycle time, must be adjusted to maximize the signal-to-noise ratio (column 1, lines 56-58 of Bianchi). Therefore, it would have been obvious to combine Bianchi with Zhou in view of Tachiuchi to obtain the invention as specified in claim 5.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A. Thompson whose telephone number is 571-272-7441. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James A. Thompson
Examiner
Art Unit 2624

JAT
28 April 2005

THOMAS D. LEE
PRIMARY EXAMINER